REMARKS

Claims 13, 14, 16-17, and 41-42 are pending in the present application. Claims 13 and 42 have been amended. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A. Applicants respectfully request reconsideration of all rejections in light of the amendments and following remarks.

Claims 13 and 42 have been amended to recite in pertinent part a ratio "from approximately 0.1 to approximately 0.80 of hydrogen gas to oxygen gas." Support for this recitation is found in the specification at page 8, lines 18-20.

Claims 13, 16-17, and 42 stand rejected under 35 U.S.C. §102 as being anticipated by Luan, et al. "Ultra Thin High Quality Ta_2O_5 Gate Dielectric Prepared by *In-situ* Rapid Thermal Processing" IEEE '98 Technical Digest, pp. 609-612 ("Luan"). Reconsideration is respectfully requested.

Claim 13 recites a method of fabricating a semiconductor device including "depositing a dielectric film over an active region . . . and subjecting the dielectric film to a wet oxidation with steam provided by heating a mixture of hydrogen and oxygen gases . . . said mixture is a ratio from approximately 0.1 to approximately 0.80 of hydrogen gas to oxygen gas."

Similarly, claim 42 recites "depositing a dielectric film . . . to form one of a gate and a capacitor dielectric, and subjecting the dielectric film to a wet oxidation with steam provided by heating a mixture of hydrogen and oxygen gases . . . said mixture is a ratio from approximately 0.1 to approximately 0.80 of hydrogen gas to oxygen gas."

Luan does not anticipate Applicants' claimed invention. Although Luan may teach an *in-situ* RTP processing of a gate dielectric, Luan specifically discloses an "*in-situ* multiprocessing *with* [an] NO surface passivation layer." (Leakage Current, 2).

Further, Luan is void of any teaching of "subjecting the dielectric film to a *wet oxidation* with steam provided by heating a mixture of hydrogen and oxygen gases . . . said *mixture is a ratio* from approximately *0.1 to approximately 0.80* of hydrogen gas to oxygen gas," as recited in claims 13 and 42 (emphasis added).

Claims 16-17 depends from and contains all of the limitations of claim 13. For at least these reasons, claims 16-17 are similarly allowable along with claim 13.

Accordingly, withdrawal of the rejection for claims 13, 16-17, and 42 is solicited.

Claims 14 and 41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Luan in view of Tseng et al. (U.S. Patent No. 6,063,698) ("Tseng"). Reconsideration is respectfully requested.

At the outset, Applicants note that the arguments provided above regarding independent claim 13 is equally applicable here. Dependent claim 14 incorporates all of the limitations of claim 13. Accordingly, dependent claim 14 is similarly allowable for the reasons set forth above regarding independent claim 13.

Claim 41 further recites a method for fabricating a semiconductor device including "depositing a dielectric film with a thickness greater than about 40 Angstroms . . . and subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature greater than about 450 °C."

Whereas, Tseng teaches a method of forming an "improved gate dielectric for a polysilicon-gated transistor . . . having reduced trap sites, and reduced substrate plasma damage." (Col. 3, lines 9-12). Specifically, Tseng's wet oxidation method requires "*specific hydrogen concentrations*, whereby the benefit of reducing substrate plasma damage . . . trap bulk sites . . . and interface trap sites . . . are realized." (Col. 4, lines 1-6). Further, "[t]he percentage of H_2 in the O_2 and H_2 mixture [is] approximately 6%." (Col. 6, lines 60-61).

Applicants respectfully submit that there is no motivation to combine Tseng with Luan. In Luan, "a high quality interfacial layer *is required* for Ta_2O_5 gate dielectrics on Si . . . [it] provides a good interface . . . [and it] also *prevent*[s] the *Si surface* from being *oxidized* during Ta_2O_5 CVD deposition *as well as* during post-deposition annealing." (Results and Discussion, 1) (emphasis added). Thus, Luan's "NO passivation layer is stable, i.e., *not being oxidized* during CVD Ta_2O_5 deposition." (Results and Discussion, 1) (emphasis added).

Tseng teaches that "exposure to the wet oxidation environment will result in oxidation consumption of . . . the substrate which underlies the oxide." (Col. 5, lines 65-67). Therefore, the "thermal oxidation of the substrate will consume, via substrate oxidation," portions of a plasma etch damage as a result of etching the polysilicon gate (Col. 6, lines 8-10).

The silicon surface in Luan is <u>prevented</u> from being oxidized by the NO passivation layer. In contrast, Tseng teaches oxidizing the silicon substrate layer to repair plasma etch damage. The presence and resistance of Luan's NO passivation layer to oxygen oxidation allows fabrication of a thinner high-K dielectric. Accordingly, the methods in Tseng cannot be combined with Luan.

Further, Luan illustrates in FIGS. 2, 4, and 6, a Ta_2O_5/Al gate. Tseng discloses that it is not possible to perform an oxidation step to cure plasma etch damage when a metal gate is employed. "At temperatures higher than 520°C . . . aluminum gates would be destroyed, degraded, severely oxidized ." (Col. 3, lines 1-8). Accordingly, the cited references are not combinable due to thermal constraints.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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